Yanagisawa provides a phase difference detector for detecting a phase difference between two input signals, and a jitter detector and method for detecting the amount of jitter between the two input signals. The jitter detector obtains a digital phase difference value between the two input signals. A comparison pulse generator outputs a series of phase difference comparison pulses. A periodic signal generator outputs a periodic signal every time a value obtained by accumulating the widths of the phase difference comparison pulses exceeds a predetermined value. A counter counts the number of pulses of the clock signal and an arithmetic unit detects and outputs a variation in the count as jitter between the first and second input signals.

Regarding claim 1, the Applicant respectfully traverses the rejection on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

> "converting the delay value to an edge position output; and
> detecting a value of the edge position output."

The Examiner states in the Office Action dated April 25, 2005:

> "Although Kelkar et al does not disclose converting the delay value to an edge position and detecting a value of the edge position, Yanagisawa et al discloses an edge detector converts (sic) the first and second signal into first and second timing signals, a comparison pulse generator that outputs the phase difference or delay value of the first and second timing signals. (Fig. 7, labels 107 and 103)" [underlining for clarity]

However, Kelkar does not show outputting first and second input signals as would be required for the input for Yanagisawa because Kelkar, column 3, lines 48-50, states:

> "The output 17 of the edge sorting circuit 12 is an N-1 bit word ... for each measured transition edge." [deletions and underlining for clarity]

The above shows that Kelkar's output is a series of single output values, not a pair of parallel signals as required as input by Yanagisawa.

Yanagisawa, as shown in FIG. 7 and described at column 8, lines 39-43, states:

> "Receiving the first and second input signals 101 and 102, the edge detector 107 converts the first and second input signals 101 and 102 into first and second timing signals 1011 and 1021 and then outputs the signals 1011 and 1021 to the comparison pulse generator 103." [underlining for clarity]

These signals are received and transmitted in parallel, as shown in FIG. 7, to the comparison pulse generator, as described in column 9, lines 7-9 of Yanagisawa:

> "The comparison pulse generator 103 outputs the phase difference between the first and second timing signals 1011 and 1021..."

Thus, in the hypothetical combination proposed by the Examiner, Yanagisawa is not receiving a delay value and converting it to an edge position, and then detecting a value of that (single) edge position as called for in claim 1:

> "converting the delay value to an edge position output; and
> detecting a value of the edge position output."

Thus, to substitute Yanagisawa into Kelkar would require Kelkar to output two parallel input signals to Yanagisawa for Yanagisawa's two input signals. Kelkar provides no such output. Thus, the references cannot be combined, and such a combination would be inoperative.

Accordingly, and based upon the above, it is respectfully submitted that claim 1 is allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because, where the references as a whole teach away from each other and would produce an inoperative device, the combination taken as a whole cannot be obvious because the CAFC has stated:

> "We have noted elsewhere, as a "useful general rule," that references that teach away cannot serve to create a prima facie case of obviousness... If references taken in combination would produce a "seemingly inoperative device", we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1354 (Fed. Cir. 2001). [deletion for clarity]

Accordingly, withdrawal of the rejection of claim 1 is respectfully requested.

Regarding claim 4, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

The Applicant also respectfully traverses the rejection of claim 4 on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of

Yanagisawa since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

> "analyzing the edge position output to determine edge position movement in excess of a predetermined magnitude." [underlining for clarity]

The Examiner states in the Office Action:

> "Yanagisawa et al discloses a comparator comparing the phase different or edge movement exceeding a predetermined value. (Abstract, lines 9-12)"

However, Yanagisawa does not show determining edge position movement in excess of a predetermined magnitude because Yanagisawa, Abstract, lines 8-12, states:

> "The periodic signal generator outputs a periodic signal every time a value obtained by accumulating the widths of the phase difference comparison pulses exceeds a predetermined value." [underlining for clarity]

The above shows that Yanagisawa is accumulating multiple values, and thus neither describes nor suggests analyzing the edge position output to determine edge position movement in excess of a predetermined magnitude, as called for in claim 4.

Accordingly, and based upon the above, it is respectfully submitted that claim 4 is allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Accordingly, withdrawal of the rejection of claim 4 is respectfully requested.

Claims 2, 5-7, 9-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar"), in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), and further in view of Sunter et al. (US Application No. 20050069031, hereinafter "Sunter").

Kelkar and Yanagisawa were previously summarized above.

Sunter measures a statistical value of jitter for a data signal. The data signal is digitally sampled to produce sampled logic values, and the sampled values are analyzed to deduce a statistical value of the jitter.

Regarding claim 2, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Further with regard to claim 2, if the rejection is maintained, the Examiner is respectfully requested to clarify the reference to "Col. 15, lines 26-28" of Sunter. The Applicant was unable to locate this portion of Sunter and is therefore unable to address this rejection further.

Regarding claim 5, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Further with regard to claim 5, the Applicant also respectfully traverses the rejection of this claim on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa and further in view of Sunter since the Applicant's claimed combination includes the limitation of:

"analyzing the edge position output to provide a root mean square value thereof"

The Examiner states in the Office Action:

> "Sunter et al inherently discloses the calculation of the root mean square by measuring a statistical value of the output data computed by the analysis circuitry. (page 2, paragraph [0017] and Fig. 6A, label 22)"

However, Sunter does not teach calculation of the root mean square as stated by the Examiner because label 22 is not defined in the disclosure, and page 2, paragraph [0017] states:

> "[0017] One aspect of the present invention is generally defined as a circuit for measuring a statistical value of jitter for a data signal having a data rate, f_D, the circuit comprising a clock generator for generating a clock signal having a rate, f_S, where f_D/f_S is a constant non-integer ratio; digital latching

> circuitry for latching the data signal using the clock; and analysis circuitry for computing jitter based on output data of the latching circuitry and the values of f_D and f_S."

The above neither teaches nor describes calculation of the root mean square. Withdrawal of the rejection of claim 5 is therefore respectfully requested because, as indicated in MPEP §2112:

> "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re* Rijckaert, 9 F.3d 1531, 1534, 28 USPQ 2d 1955, 1957 (Fed. Cir. 1993)(reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art)."

Regarding claim 6, the Applicant respectfully traverses the rejection on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa and further in view of Sunter since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

> "converting the delay value to an edge position output using the sampling clock signal;
> detecting peak-to-peak values of the edge positions;"

These same issues with regard to the lack of a parallel output from Kelkar and the required parallel input to Yanagisawa, for the first and second input signals 101 and 102, have been discussed in detail above with respect to the rejection of claim 1, and those arguments are equally applicable to the rejection of claim 6. Consequently, the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa and further in view of Sunter. On those same bases, therefore, the Applicant respectfully traverses the rejection of claim 6.

Accordingly, and based on the above, since there is no teaching or motivation in these references for the hypothetical combination of Kelkar in view of Yanagisawa and further in view of Sunter, as suggested by the Examiner, it is respectfully submitted that claim 6 is allowable under 35 USC §103 as being unobvious at the time the invention was made to a person having ordinary skill in the art. McGinley, quoted above.

Claim 7 was rejected on the grounds that it inherits all the limitations of claim 2.

Regarding claim 7, this dependent claim depends from independent claim 6 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 7 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 2.

Claim 9 was rejected on the grounds that it inherits all the limitations of claim 4.

Regarding claim 9, this dependent claim depends from independent claim 6 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 9 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 4.

Claim 10 was rejected on the grounds that it inherits all the limitations of claim 5.

Regarding claim 10, this dependent claim depends from independent claim 6 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 10 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 5.

Regarding claim 11, the Applicant respectfully traverses the rejection on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa and further in view of Sunter since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

"a priority encoder connected for converting the signal transition location to a delay value;

a converter connected for converting the delay value to an edge position output"

These same issues with regard to the lack of a parallel output from Kelkar and the required parallel input to Yanagisawa, for the first and second input signals 101 and 102, have been discussed in detail above with respect to the rejection of claim 1, and those arguments are equally applicable to the rejection of claim 11. Consequently, the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa and further in view of Sunter. On those same bases, therefore, the Applicant respectfully traverses the rejection of claim 11.

Accordingly, and based on the above, since there is no teaching or motivation in these references for the hypothetical combination of Kelkar in view of Yanagisawa and further in view of Sunter, as suggested by the Examiner, it is respectfully submitted that claim 11 is allowable under 35 USC §103 as being unobvious at the time the invention was made to a person having ordinary skill in the art. McGinley, quoted above.

Claim 12 was rejected on the grounds that it inherits all the limitations of claim 2.

Regarding claim 12, this dependent claim depends from independent claim 11 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 12 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 2.

Claim 14 was rejected on the grounds that it inherits all the limitations of claim 4.

Regarding claim 14, this dependent claim depends from independent claim 11 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 14 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 4.

Claim 15 was rejected on the grounds that it inherits all the limitations of claim 5.

Regarding claim 15, this dependent claim depends from independent claim 11 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 15 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 5.

Claims 16-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar"), in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Application No. 20050069031, hereinafter "Sunter"), and further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial" (hereinafter "IEEE").

Regarding claim 16, the Applicant respectfully traverses the rejection on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of IEEE, since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

> "a priority encoder connected for converting the data signal transition location to a delay value;
> a converter for converting clock and delay to time values and connected for converting the delay value to an edge position output;"

These same issues with regard to the lack of a parallel output from Kelkar and the required parallel input to Yanagisawa, for the first and second input signals 101 and 102, have been discussed in detail above with respect to the rejection of claim 1, and those arguments are equally applicable to the rejection of claim 16. Consequently, the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of IEEE. On those same bases, therefore, the Applicant respectfully traverses the rejection of claim 16.

Accordingly, and based on the above, since there is no teaching or motivation in these references for the hypothetical combination of Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of IEEE, as suggested by the Examiner, it is respectfully

submitted that claim 16 is allowable under 35 USC §103 as being unobvious at the time the invention was made to a person having ordinary skill in the art. McGinley, quoted above.

Claim 17 was rejected on the grounds that it inherits all the limitations of claim 2.

Regarding claim 17, this dependent claim depends from independent claim 16 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 17 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 2.

Claim 19 was rejected on the grounds that it inherits all the limitations of claim 4.

Regarding claim 19, this dependent claim depends from independent claim 16 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 19 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 4.

Claim 20 was rejected on the grounds that it inherits all the limitations of claim 5.

Regarding claim 20, this dependent claim depends from independent claim 16 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 20 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 5.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar"), in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), and further in view of Suzuki (US Patent No. 6,782,353, hereinafter "Suzuki").

Regarding Claim 3, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

The Applicant also respectfully traverses the rejection of claim 3 on the grounds that the Applicant's claimed combination would not be unpatentable over Kelkar in view of Yanagisawa, and further in view of Suzuki, since the Applicant's claimed combination includes the limitation not disclosed in Suzuki of:

> "adding a dither signal to the signal under test prior to inputting the signal under test to generate signal transition locations"

The Examiner states in the Office Action:

> "Suzuki discloses an OR circuit adding the delay signal outputted by the delay circuit to the data signal. (Fig. 11, labels 12b, 12a and Col. 2, lines 6-16)"

However, Suzuki does not teach or suggest adding a dither signal because Suzuki, column 2, lines 21-23, states:

> "The output shown in FIG. 10D is a signal where pulses are inserted one by one in each period in which a pulse train is not outputted in FIG. 10B."

The above shows that Suzuki's OR circuit is merely filling in pulses when they are otherwise missing during the absence of a pulse train. This is not the addition of a dither signal and has nothing to do with the dither signal as disclosed, defined, and claimed in the present invention. Accordingly, and based upon the above, it is respectfully submitted that claim 3 is allowable on this ground as well under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because of *In re* Vaeck, *supra*.

Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar"), in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Application No. 20050069031, hereinafter "Sunter"), and further in view of Suzuki (US Patent No. 6,782,353, hereinafter "Suzuki").

Claims 8 and 13 were rejected on the grounds that they inherit all the limitations of claim 3.

Regarding claims 8 and 13, these dependent claims depend from respective independent claims 6 and 11 and are believed to be allowable since they contain all the limitations set forth in the respective independent claims from which they depend and claim unobvious combinations thereof.

Claim 8 and 13 are also believed to be allowable since they are similarly distinguished from the limitations that were asserted with respect to claim 3.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar"), in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Application No. 20050069031, hereinafter "Sunter"), further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial", and further in view of Suzuki (US Patent No. 6,782,353, hereinafter "Suzuki").

Claim 18 was rejected on the grounds that it inherits all the limitations of claim 3.

Regarding claim 18, this dependent claim depends from independent claim 16 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof.

Claim 18 is also believed to be allowable since it is similarly distinguished from the limitations that were asserted with respect to claim 3.